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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/724,989 | 12/01/2003 | Visvesvaraya A. Pentakota | TI-37261 | 1873 |

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| EXAMINER | |
|---|---|
| TON, MY TRANG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2816 | |

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/724,989 | PENTAKOTA ET AL. |
| | Examiner | Art Unit |
| | My-Trang N. Ton | 2816 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *6,7,10,11,18,19,22 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6,7,18 and 19* is/are allowed.

6)☒ Claim(s) *10,11,22 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-11, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Flannagan (U.S Patent No. 6,031,408) and further in view of Li (U.S. Patent No. 6,836,160).

Flannagan discloses in Fig. 6 a square low clamping circuit including:

Regarding claim 10:

a first transistor (132) designed to be turned on when the voltage level is outside of the specified range (when 132 ON); and

a current amplifier (135 and 136) drawing a substantial amount of current from the node (121) when the first transistor is turned on (132 ON), which causes the voltage level at the node (121) to be pulled to within the specified range;

biasing circuit (130, 131, 133, 134) generating a bias signal to a gate terminal of the first transistor (132), wherein a voltage level of the bias signal is determined by an upper limit or a lower limit of the specified range,

wherein the current amplifier (135, 136) comprises:

a second transistor (135) and a third transistor (136), wherein a gate terminal of the third transistor (136) is connected to both drain and gate terminals of the second

transistor (135), a source terminal of the third transistor (136) is connected to ground (Vss), the drain terminal of the second transistor (135) is connected to a drain terminal of the first transistor (132), and a drain terminal of the third transistor (136) is connected to a source terminal of the first transistor (132).

However, this reference does not specifically disclose "a resistor connected between a source terminal of said second transistor and ground" as recited in claim 10.

Li teaches well-known limitation in the art for providing higher resistance and providing more voltage drop in the circuit by having a resistor between the source of the transistor and ground: for example: resistor R1 connected between QN and ground (via R2).

Therefore, it would have been obvious at the time the invention was made for one skilled in the art to use the teaching as taught in Li for the Flannagan's reference by inserting the resistor between a source terminal of the second transistor (135) and ground (Vss) for the purpose of providing more voltage drop and higher resistance.

Regarding the limitation of claim 11: each of the second transistor and the third transistor comprises a NMOS transistor (135-136).

Claims 22-23 are similarly rejected as claims 10-11.

***Allowable Subject Matter***

Claims 6-7 and 18-19 are allowable over the prior art of record.

None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: "a gate terminal of said

second transistor receiving a second bias voltage" in combination with "the first transistor", the details of "the current amplifier" and "the biasing circuit" as recited in claims 6 and 18.

***Response to Arguments***

Applicant's arguments filed 12/16/05 have been fully considered but they are not persuasive.

Applicant's argument – Applicant requests a teaching from the prior art.

Examiner's response - As shown in Li, resistor R1 connected between QN and ground (via R2) is notoriously well known construction in the art. Because of the well-known advantages in performance, the skill artisan would have been motivated to insert resistor between a source terminal of the second transistor (135) and ground of Flannagan since this construction is deemed conventional.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton
Primary Examiner
Art Unit 2816

February 21, 2006